REMARKS

In accordance with the foregoing, claims 1-48 are now pending and under consideration. Claims 1, 3, 7, 10, 12, 13, 16, 17, 25 and 31 have been amended and claims 37-48 have been added. No new matter is included in this Amendment.

The 35 U.S.C. §102(e) Rejection

At page 3 of the Office Action, claims 1, 4, 7, 11, 12, 14, 15 and 25-36 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,233,394 to Jeong et al.

The Examiner asserts that Jeong et al. discloses a demodulator performing EFM+ in a DVD mode (212) and EFM in a CD mode (214). Admittedly, Jeong et al. includes features for demodulating both an ESM signal and an EFM signal. However, in Jeong et al., separate demodulators are used for ESM and EFM signals as indicated by the separate reference characters 212 and as described at col. 3, lines 44-46, "a switch 297 provides for separate DVD and CD processing according to a first disc identification signal disc 2 provided by the microcomputer (micro) 500." Thus, Jeong et al. fails to disclose "a single demodulator to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and EFM demodulate the pulse stream according to the symbol clock in a CD mode, to generate demodulated data," as claimed in amended claim 1. Further, independent claims 7, 12, 25 and 31 have also been amended to incorporate the feature of the single demodulator. Thus, claims 7, 12, 25 and 31 are deemed to be patentable over Jeong et al. at least for similar reasons set for the above regarding claim 1. Claim 4 is deemed to be patentable at least for similar reasons set forth above regarding claim 1. Claim 11 is deemed to be patentable at least for similar reasons set forth above regarding claim 7. Claims 14 and 15 are deemed to be patentable at least for similar reasons set forth above regarding claim 12. Claims 26-30 are deemed to be patentable at least for similar reasons set forth above regarding claim 25 and claims 32-35 are deemed to be patentable at least for similar reasons set forth above regarding claim 31.

STATEMENT CONCERNING COMMONLY OWNED SUBJECT MATTER

The present application and the subject matter of U.S. Patent 6,233,394 to Jeong et al. were, at the time the invention was made, owned by or subject to an obligation of

assignment to Samsung Electronics Co., Ltd.

A Continued Prosecution Application, of which this Preliminary Amendment is a part, has been filed, thus the present application becomes an application filed after November 29, 1999 and is entitled to the benefits of 35 U.S.C. §103(c) regarding commonly owned subject matter. Thus, U.S. Patent 6,233,394 to Jeong et al. may not be used as a reference in a rejection under 35 U.S.C. §103(a).

The First 35 U.S.C. §103(a) Rejection

At page 4 of the Office Action, claims 2-3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,233,394 to Jeong et al. in view of U.S. Patent 6,119,262 to Chang et al. In view of the statement of common ownership set for the above, U.S. Patent 6,233,394 is not a valid reference for a rejection under 35 U.S.C. 103(a). Therefore, it is respectfully requested that the rejection of claims 2-3 and 10 be withdrawn.

The Second 35 U.S.C. §103(a) Rejection

At page 5 of the Office Action, claims 5-6, 8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,233,394 to Jeong et al. in view of U.S. Patent 5,988,872 to Jeong. In view of the statement of common ownership set for the above, U.S. Patent 6,233,394 is not a valid reference for a rejection under 35 U.S.C. 103(a). Therefore, it is respectfully requested that the rejection of claims 5-6, 8 and 13 be withdrawn.

The Third 35 U.S.C. §103(a) Rejection

At page 6 of the Office Action, claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,233,394 to Jeong et al. in view of U.S. Patent 5,988,872 to Jeong and U.S. Patent 5,970,208 to Shim. In view of the statement of common ownership set for the above, U.S. Patent 6,233,394 is not a valid reference for a rejection under 35 U.S.C. 103(a). Therefore, it is respectfully requested that the rejection of claim 9 be withdrawn.

The Fourth 35 U.S.C. §103(a) Rejection

At page 6 of the Office Action, claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,233,394 to Jeong et al. in view of U.S. Patent 6,119,262 to Chang et al. In view of the statement of common ownership set for the above, U.S. Patent 6,233,394 is not a valid reference for a rejection under 35 U.S.C. 103(a). Therefore, it is respectfully requested that the rejection of claims 16-19 be withdrawn.

The Fifth 35 U.S.C. §103(a) Rejection

At page 7 of the Office Action, claims 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,233,394 to Jeong et al. in view of U.S. Patent 5,587,981 to Kamatani. In view of the statement of common ownership set for the above, U.S. Patent 6,233,394 is not a valid reference for a rejection under 35 U.S.C. 103(a). Therefore, it is respectfully requested that the rejection of claims 20-24 be withdrawn.

Claim Amendments:

In claims 1, 3, 10, 12, 13 and 16, references to an "ECC (error checking and correction) demodulator" have been changed to --ECC (error checking and correction) decoder--, to improve form and to better coordinate with the terminology of the specification.

New Claims:

New claims 37 and 39 correspond to original claims 2 and 5, respectively which have been written in independent form to include all the features of original claim 1. Original claims 2, 3, 5 and 6 were rejected under 35 U.S.C. 103(a) in view of U.S. Patent 6,233,394 to Jeong et al. as the primary reference. Since U.S. Patent 6,233,394 to Jeong et al. is not a valid reference under 35 U.S.C. 103(a), claims 37-40 are deemed to be patentable over the prior art of record.

New claims 41 and 43 correspond to original claims 8 and 10, respectively, which have been written in independent form to include all the features of original claim 7. Original claims 8-10 were rejected under 35 U.S.C. 103(a) in view of U.S. Patent 6,233,394 to Jeong et al. as the primary reference. Since U.S. Patent 6,233,394 to Jeong et al. is not a valid reference under 35 U.S.C. 103(a), claims 41-43 are deemed to be patentable over the prior art of record.

New claim 44 corresponds to original 13, respectively which has been written in independent form to include all the features of original claim 12. Original claim 13 was rejected under 35 U.S.C. 103(a) in view of U.S. Patent 6,233,394 to Jeong et al. as the primary reference. Since Jeong et al. is not a valid reference under 35 U.S.C. 103(a), claim 44 deemed to be patentable over the prior art of record.

New claim 45 recites a combination of "a single demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively; an external memory to store the first and second demodulated data; and a single ECC (error checking and correction) decoder to error correct

the first and second demodulated data stored in said memory." The prior art does not disclose a combination as recited in new claim 45. Claims 46-48 are deemed to be patentable at least for similar reasons set forth above regarding claim 45.

Summary:

If there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: 1/9/03

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please AMEND claims 1, 3, 7, 10, 12, 13, 16, 17, 25 and 31 as shown below. Claims 2, 4-6, 8, 9, 11, 14, 15, 18-24, 26-30 and 32-36 are not amended herein but are presented in order for the convenience of the Examiner.

1. (ONCE AMENDED) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process a pulse stream of data from a DVD or a CD, comprising:

a PLL (Phase Locked Loop) to receive the pulse stream, to generate a PLL clock;

a frame/ID (identification) synchronization detector to latch the pulse stream according to said PLL clock, to generate a symbol clock;

a single demodulator to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and EFM demodulate the pulse stream according to the symbol clock in a CD mode, to generate demodulated data;

a memory to store the demodulated data from said demodulator;

an ECC (error checking and correction) [demodulator] decoder to error-correct the demodulated data stored in said memory according to a predetermined code length and error correction range, the predetermined code length and error correction range having different values in the DVD and CD modes, to generate error corrected data;

a descrambler to descramble the error corrected data stored in said memory, in the DVD mode; and

a CD audio processor to process the error corrected data stored in said memory, in the CD mode.

2. (ONCE AMENDED) The combined DVD/CD data processor as claimed in claim 1, wherein the predetermined code length and error correction range in the DVD mode are PI(182,172), PO(208,192), and the predetermined code length and error correction range in the CD mode are C1(32,28), C2(28,24).

3. (ONCE AMENDED) The combined DVD/CD data processor as claimed in claim 2, wherein said ECC [demodulator] decoder comprises:

a syndrome generator to receive said demodulated data from said memory to generate a

syndrome polynomial according to said code length and correction range of PI(182,172), PO(208,192) in the DVD mode, and of C1(32,28), C2(28,24) in the CD mode;

an erasure constant generator to receive an erasure flag to generate an erasure constant;

a modified syndrome calculator to receive the syndrome polynomial and the erasure constant to calculate a modified syndrome and generate a Forney syndrome polynomial and an erasure polynomial;

a modified Euclidean algorithm to process the Forney syndrome polynomial and the erasure polynomial based on a modified Euclidean algorithm, to generate an errata locator polynomial and an errata evaluator polynomial; and

a Chien search and error correction circuit to correct errors of the demodulated data stored in said memory according to said errata locator polynomial and said errata evaluator polynomial.

4. The combined DVD/CD data processor as claimed in claim 1, wherein said memory is an external memory.

5. The combined DVD/CD processor as claimed in claim 1, wherein said memory has a first memory map including a plurality of blocks of the error corrected data each having a first fixed number of bytes in the DVD mode, and a second memory map including a plurality of frames of the error corrected data each having a second fixed number of bytes in the CD mode.

6. The combined DVD/CD processor as claimed in claim 5, wherein:

the plurality of blocks is 13;

the first fixed number of bytes is 32.25Kbytes;

the plurality of frames is 256; and

the second fixed number of bytes is 32bytes.

7. (ONCE AMENDED) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks;

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

a single demodulator to perform a first type of demodulation on the first pulse stream according to the first symbol clock to generate first demodulated data of a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate second demodulated data of a CD mode;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) [demodulator] decoder to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range and to store the error corrected first demodulated data back in said memory, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range and to store the error corrected second demodulated data back in said memory.

8. The combined DVD/CD data processor as claimed in claim 7, wherein said memory comprises:

a first memory map to store the error corrected second demodulated data; and

a second memory map different from the first memory map, to store the error corrected second demodulated data.

9. The combined DVD/CD data processor as claimed in claim 8, wherein said first memory map provides a VBR (variable bit rate) control margin to interface the error corrected first demodulated data with an audio/video decoder.

10. (ONCE AMENDED) The combined DVD/CD data processor as claimed in claim 7, wherein said ECC [demodulator] decoder comprises:

a syndrome generator to generate syndrome polynomials from the first and second demodulated data stored in said memory in accordance with the corresponding first and second code lengths and corresponding first and second correction ranges;

an erasure constant generator to generate first and second erasure constants from corresponding first and second erasure flags;

a modified syndrome calculator to generate first and second Forney syndrome

polynomials and first and second erasure polynomials from the corresponding first and second erasure constants and the corresponding syndrome polynomials;

a modified Euclidean algorithm to process the first and second Forney syndrome polynomials with the corresponding first and second erasure polynomials, to generate corresponding first and second errata locator polynomials and corresponding first and second errata evaluator polynomials; and

a Chien search and error correction unit to correct errors of the first and second demodulated data stored in said memory according to the corresponding first and second errata locator polynomials and the corresponding first and second errata evaluator polynomials.

11. The combined DVD/CD data processor as claimed in claim 7, further comprising:

a descrambler to descramble the error corrected first demodulated data stored in said memory for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data stored in said memory.

12. (ONCE AMENDED) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a single demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) [demodulator] decoder to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range in the DVD mode, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range in the CD mode.

13. (ONCE AMENDED) The combined DVD/CD data processor as claimed in claim 12, wherein said memory stores the error corrected first demodulated data output from said ECC [demodulator] decoder in a first memory map, and the error corrected second demodulated data output from said ECC [demodulator] decoder in a second memory map different from the first memory map.

14. The combined DVD/CD data processor as claimed in claim 12, further comprising:

a descrambler to descramble the error corrected first demodulated data stored in said memory for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data stored in said memory.

15. The combined DVD/CD data processor as claimed in claim 12, further comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks; and

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

wherein said demodulator performs a first type of demodulation on the first pulse stream according to the first symbol clock to generate the first demodulated data in the DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate the second demodulated data in the CD mode.

16. (ONCE AMENDED) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

a single external memory to store the first and second demodulated data; and

a single ECC (error checking and correction) [demodulator] decoder to error correct the first and second demodulated data stored in said memory.

17. (ONCE AMENDED) The combined DVD/CD as claimed in claim 16, wherein said single ECC [demodulator] decoder error corrects the first and second demodulated data stored in said memory in accordance with corresponding different code lengths and correction ranges.

18. The combined DVD/CD data processor as claimed in claim 16, further comprising:

a descrambler to descramble the error corrected first demodulated data for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data.

19. The combined DVD/CD data processor as claimed in claim 16, further comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks; and

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

wherein said demodulator performs a first type of demodulation on the first pulse stream according to the first symbol clock to generate the first demodulated data in a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate the second demodulated data in a CD mode.

20. A data processor apparatus for common use in a DVD (Digital Video Disk)/CD (Compact Disk) player using discrimination information provided according to a DVD or a CD, comprising:

a signal pre-processor generating a clock from a pulse stream read from one of the DVD and the CD and performing demodulation of the pulse stream according to the discrimination information and the generated clock;

a memory unit storing the demodulated pulse stream processed by the signal pre-processor as data in a corresponding format according to the discrimination information; and

a data processor and converter processing the data stored in the memory unit.

21. The data processor apparatus as claimed in claim 20, wherein the data processor and converter audio-converts or data-converts the processed data according to the discrimination information.

22. The data processor apparatus as claimed in claim 20, wherein the data processor and converter comprises an error corrector error-correcting the data stored in the memory unit according to the discrimination information using a preset error correcting method.

23. The data processor apparatus as claimed in claim 22, wherein the preset error correcting method of the error corrector depends on a code length and a correcting range according to the discrimination information.

24. The data processor apparatus as claimed in claim 20, wherein the memory unit comprises:

a data storage memory; and

a memory controller controlling the memory to store the data in the corresponding format according to the discrimination information.

25. (ONCE AMENDED) A data processor apparatus for sharing a memory according to discrimination information which depends on a type of an information storage medium which stores data, comprising:

a [signal] single pre-processor performing demodulation of the data according to the discrimination information;

a memory unit storing the demodulated data processed by the signal pre-processor in a corresponding format according to the discrimination information; and

a data processor and converter processing the data stored in the memory unit.

26. The data processor apparatus as claimed in claim 25, wherein the signal pre-processor generates a clock from a pulse stream read from the information storage medium.

27. The data processor apparatus as claimed in claim 25, wherein the data processor and converter audio-converts or data-converts the processed data according to the discrimination information.

28. The data processor apparatus as claimed in claim 25, wherein the data processor and converter comprises an error corrector error-correcting the data stored in the memory unit according to the discrimination information using a preset error correcting method.

29. The data processor apparatus as claimed in claims 28, wherein the preset error correcting method of the error corrector depends on a code length and a correcting range according to the discrimination information.

30. The data processor apparatus as claimed in claim 25, wherein the memory unit comprises:

a data storage memory; and

a memory controller controlling the memory to store the data in the corresponding format according to the discrimination information.

31. (ONCE AMENDED) An optical disk drive, comprising:

a controller determining a type of a disk through a signal read from the disk and outputting discrimination information according to the disk type;

a [signal] single pre-processor performing demodulation of data from the disk according to the discrimination information;

a memory unit storing the demodulated data processed by the signal pre-processor in a corresponding format according to the discrimination information;

a data processor and converter processing the data stored in the memory unit.

32. The optical disk drive as claimed in claim 31, wherein the signal pre-processor generates a clock from a pulse stream read from the disk.

33. The optical disk drive as claimed in claim 31, wherein the data processor and converter audio-converts or data-converts the processed data according to the discrimination information.

34. The optical disk drive as claimed in claim 31, wherein the data processor and converter comprises an error corrector error-correcting the data stored in the memory unit according to the discrimination information using a preset error correcting method.

35. The optical disk drive as claimed in claim 34, wherein the preset error correcting method of the error corrector depends on a code length and a correcting range according to the discrimination information.

36. The optical disk drive as claimed in claim 31, wherein the memory unit comprises:

a data storage memory; and

a memory controller controlling the memory to store the data in the corresponding format according to the discrimination information.

Please ADD claims 37-48 as follows:

37. (NEW) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process a pulse stream of data from a DVD or a CD, comprising:

a PLL (Phase Locked Loop) to receive the pulse stream, to generate a PLL clock;

a frame/ID (identification) synchronization detector to latch the pulse stream according to said PLL clock, to generate a symbol clock;

a demodulator to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and EFM demodulate the pulse stream according to the symbol clock in a CD mode, to generate demodulated data;

a memory to store the demodulated data from said demodulator;

an ECC (error checking and correction) decoder to error-correct the demodulated data stored in said memory according to a predetermined code length and error correction range, the predetermined code length and error correction range having different values in the DVD and CD modes, to generate error corrected data, wherein the predetermined code length and error correction range in the DVD mode are PI(182,172), PO(208,192), and the predetermined code length and error correction range in the CD mode are C1(32,28), C2(28,24);

a descrambler to descramble the error corrected data stored in said memory, in the DVD mode; and

a CD audio processor to process the error corrected data stored in said memory, in the CD mode.

38. (NEW) The combined DVD/CD data processor as claimed in claim 37, wherein said ECC decoder comprises:

a syndrome generator to receive said demodulated data from said memory to generate a syndrome polynomial according to said code length and correction range of PI(182,172), PO(208,192) in the DVD mode, and of C1(32,28), C2(28,24) in the CD mode;

an erasure constant generator to receive an erasure flag to generate an erasure constant;

a modified syndrome calculator to receive the syndrome polynomial and the erasure constant to calculate a modified syndrome and generate a Forney syndrome polynomial and an erasure polynomial;

a modified Euclidean algorithm to process the Forney syndrome polynomial and the erasure polynomial based on a modified Euclidean algorithm, to generate an errata locator polynomial and an errata evaluator polynomial; and

a Chien search and error correction circuit to correct errors of the demodulated data stored in said memory according to said errata locator polynomial and said errata evaluator polynomial.

39. (NEW) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process a pulse stream of data from a DVD or a CD, comprising:

a PLL (Phase Locked Loop) to receive the pulse stream, to generate a PLL clock;

a frame/ID (identification) synchronization detector to latch the pulse stream according to said PLL clock, to generate a symbol clock;

a demodulator to EFM+ demodulate the pulse stream according to the symbol clock in a DVD mode, and EFM demodulate the pulse stream according to the symbol clock in a CD mode, to generate demodulated data;

a memory to store the demodulated data from said demodulator;

an ECC (error checking and correction) decoder to error-correct the demodulated data stored in said memory according to a predetermined code length and error correction range, the predetermined code length and error correction range having different values in the DVD and CD modes, to generate error corrected data;

a descrambler to descramble the error corrected data stored in said memory, in the DVD mode; and

a CD audio processor to process the error corrected data stored in said memory, in the

CD mode,

wherein said memory has a first memory map including a plurality of blocks of the error corrected data each having a first fixed number of bytes in the DVD mode, and a second memory map including a plurality of frames of the error corrected data each having a second fixed number of bytes in the CD mode.

40. (NEW) The combined DVD/CD processor as claimed in claim 39, wherein:
the plurality of blocks is 13;
the first fixed number of bytes is 32.25 Kbytes;
the plurality of frames is 256; and
the second fixed number of bytes is 32 bytes.

41. (NEW) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks;

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

a demodulator to perform a first type of demodulation on the first pulse stream according to the first symbol clock to generate first demodulated data of a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate second demodulated data of a CD mode;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) decoder to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range and to store the error corrected first demodulated data back in said memory, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range and to store the error corrected second demodulated data back in said memory, wherein said memory comprises:

a first memory map to store the error corrected second demodulated data; and

a second memory map different from the first memory map, to store the error corrected second demodulated data.

42. (NEW) The combined DVD/CD data processor as claimed in claim 41, wherein said first memory map provides a VBR (variable bit rate) control margin to interface the error corrected first demodulated data with an audio/video decoder.

43. (NEW) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks;

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

a demodulator to perform a first type of demodulation on the first pulse stream according to the first symbol clock to generate first demodulated data of a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate second demodulated data of a CD mode;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) decoder to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range and to store the error corrected first demodulated data back in said memory, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range and to store the error corrected second demodulated data back in said memory,

wherein said ECC decoder comprises:

a syndrome generator to generate syndrome polynomials from the first and second demodulated data stored in said memory in accordance with the corresponding first and second code lengths and corresponding first and second correction ranges,

an erasure constant generator to generate first and second erasure constants from corresponding first and second erasure flags,

a modified syndrome calculator to generate first and second Forney syndrome polynomials and first and second erasure polynomials from the corresponding first and second erasure constants and the corresponding syndrome polynomials,

a modified Euclidean algorithm to process the first and second Forney syndrome polynomials with the corresponding first and second erasure polynomials, to generate corresponding first and second errata locator polynomials and corresponding first and second errata evaluator polynomials,and

a Chien search and error correction unit to correct errors of the first and second demodulated data stored in said memory according to the corresponding first and second errata locator polynomials and the corresponding first and second errata evaluator polynomials.

44. (NEW) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

a memory to store the first and second demodulated data; and

an ECC (error checking and correction) decoder to error correct the first demodulated data stored in said memory in accordance with a first predetermined code length and error correction range in the DVD mode, and to error correct the second demodulated data stored in said memory in accordance with a second predetermined code length and error correction range in the CD mode,

wherein said memory stores the error corrected first demodulated data output from said ECC decoder in a first memory map, and the error corrected second demodulated data output from said ECC decoder in a second memory map different from the first memory map.

45. (NEW) A combined DVD (Digital Video Disk)/CD (Compact Disk) data processor to process first and second pulse streams from a DVD and a CD, respectively, comprising:

a single demodulator to demodulate the first and second pulse streams in a DVD mode and a CD mode, respectively, to generate first and second demodulated data, respectively;

an external memory to store the first and second demodulated data; and

a single ECC (error checking and correction) decoder to error correct the first and second demodulated data stored in said memory.

46. (NEW) The combined DVD/CD as claimed in claim 45, wherein said single ECC decoder error corrects the first and second demodulated data stored in said memory in accordance with corresponding different code lengths and correction ranges.

47. (NEW) The combined DVD/CD data processor as claimed in claim 45, further comprising:

a descrambler to descramble the error corrected first demodulated data for use with an audio/video decoder; and

an audio processor to audio process the error corrected second demodulated data.

48. (NEW) The combined DVD/CD data processor as claimed in claim 45, further comprising:

a PLL (Phase Locked Loop) to receive the first and second pulse streams, to generate respective first and second PLL clocks; and

a frame/ID (identification) synchronization detector to latch the first and second pulse streams according to the respective first and second PLL clocks, to generate respective first and second symbol clocks;

wherein said demodulator performs a first type of demodulation on the first pulse stream according to the first symbol clock to generate the first demodulated data in a DVD mode, and a second type of demodulation on the second pulse stream according to the second symbol clock to generate the second demodulated data in a CD mode.